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scmproxy GUI Client Pdf download . Ethernet is a computer network architecture in which one or more devices or computers is connected to a source of a transmission medium, e.g., twisted-pair copper wires, and to one or more destinations (or “neighbor” devices) using a physical media access control (PMAC) sublayer or device. A station is connected to the medium through a physical layer (PHY) device. The station comprises a physical media access controller (PMAC) and one or more transceivers. The PMAC is connected to the PHY by a system bus or a network (e.g., a local area network (LAN)) connected to the PHY. The transceivers allow communication between the PHY and the system bus or the network. Each transceiver comprises an input receiver for receiving information from the medium, an output transmitter for transmitting information from the system bus or the network, and a register for storing the transceiver's operational parameters. A plurality of transceivers may be provided on a transceiver module. Each module is connected to the PMAC and to one or more network ports. The network ports connect to one or more transceiver modules. The transceiver module connects to the system bus or network. The IEEE standard for a transceiver module is 802.3ae-2003. A transceiver receives data from the medium and transmits data to the system bus or network by performing the following functions: (1) receive data from the medium, (2) transmit data to the system bus or network, (3) receive commands, (4) transmit commands, (5) read status from the PHY, (6) transmit status to the PHY, (7) transmit and receive packets, (8) pause, (9) and resume. The IEEE standard for a PMAC sublayer is IEEE 802.3z-2001. A PMAC sublayer operates by sending preamble and start of frame (SOF) characters or bits at a rate of 125 Mb/s. Referring to FIG. 1, a transceiver 100 comprises a PHY 101, a PMAC 102, a controller 103, a power supply 104, a status interface 105, a register 106, and a transceiver port 107. The PHY 101 has a receiver 110, a transmitter 112, a preamble detector 114, a retiming circuit 116, a clock domain arbitrator 118, 2d92ce491b